Remarks/Arguments

Claims 1-20 remain in this application.

The examiner has rejected claims 1-3, 5, 8, 9, 12, 14 and 20 under 35 USC 102(e) as being anticipated by *Okabe, et al.* (United States Patent 6,799,130).

The examiner has rejected claims 10 and 19 under 35 USC 103(a) as being unpatentable over *Okabe, et al.*, in view of *Matsumoto, et al.* (United States Published Patent Application 2002/0111038).

The examiner has objected to claims 4, 6, 7, 11, 13 and 15-18 as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

In view of the above amendments and these remarks, reconsideration of the above noted rejections and objections is respectfully requested.

Rejections under 35 USC 102(e):

Applicant respectfully traverses the rejection of **claims 1-3, 5, 8, 9, 12, 14 and 20** under 35 USC 102(e) as being anticipated by *Okabe, et al.* The independent claims are 1, 5, 9 and 14. Each of the independent claims calls for "points of interest" proximate to an edge of the semiconductor wafer and capturing images of the semiconductor wafer at the points of interest. (Claim 1: lines 5-6 and 9; Claim 5: lines 5-7; Claim 9: lines 7-9; Claim 14: lines 6-7.) Applicant respectfully submits that *Okabe, et al.* does not teach or suggest these limitations.

Okabe, et al. discloses defect points on the top of the wafer, within IC blocks, rather than proximate to an edge of the wafer. In particular, Figs. 3, 4, 7, 9-11 and 13 of *Okabe, et al.* show defect points 101-110, 121-135, 150 and 151 within IC chips and within circuit patterns of IC chips. (See Column 2, lines 10-19 and 56-60; Column 4, lines 4-14; Column 6, lines 41-59; Column 7, lines 52-65; Column 9, lines 49-52; Column 10, lines 5-15; Column 12, lines 11-13.) Any mention of an "edge" in

Okabe, et al. refers to 1). an outline of an LSI/circuit block or border between circuit blocks (Column 2, lines 40-48; Column 4, lines 38-47), 2). an arrangement of a chip relative to a wafer edge (Column 6, lines 48-49), 3). a position of a defect relative to an edge of a chip (Column 6, lines 56-59), or 4). an edge of a circuit pattern (Column 10, lines 25-36). *Okabe, et al.* does not discuss the defect points, however, with respect to the edge of the wafer. In other words, the disclosure in *Okabe, et al.* is similar to the brief description in the background of the present application regarding wafer top surface defect detection (p. 1, line 23, to p. 2, line 9). Applicant respectfully submits that the wafer top surface defect detection technique of *Okabe, et al.* does not teach or suggest capturing images of a semiconductor wafer at points of interest proximate to an edge of the semiconductor wafer for methods of gathering semiconductor wafer edge inspection data or a system for automated inspection of a semiconductor wafer edge as called for in the independent claims 1, 5, 9 and 14.

Applicant respectfully submits, therefore, that independent claims **1, 5, 9 and 14** are not anticipated by, are not obvious from, and are patentable over *Okabe, et al.*, since the reference does not teach or fairly suggest capturing images of a semiconductor wafer at points of interest proximate to an edge of the semiconductor wafer as claimed. Additionally, since claims 2, 3, 8, 12 and 20 depend from claims 1, 5, 9 and 14, **claims 2, 3, 8, 12 and 20** also are not anticipated by, are not obvious from, and are patentable over *Okabe, et al.* for the same reasons.

Furthermore, independent **claim 5** (lines 5-9) calls for

> generating points of interest proximate to an edge of the semiconductor wafer by identifying **fake** defects with **fake** defect identifiers;
>
> causing the review tool to capture images at the points of interest by instructing the review tool to capture the images at the **fake** defects identified by the **fake** defect identifiers...

Applicant respectfully submits that *Okabe, et al.* does not teach or suggest the limitations of fake defects and fake defect identifiers. Instead, *Okabe, et al.* refers throughout its written description to "detected defects," which are actual defects. *Okabe, et al.* also refers to "false defects," which are simply mistakenly identified as

defects (Column 2, lines 42-46; Column 4, lines 39-44). Applicant respectfully submits, therefore, that independent **claim 5** is not anticipated by, is not obvious from, and is patentable over *Okabe, et al.*, since the reference does not teach or fairly suggest fake defects, fake defect identifiers and the use thereof as claimed. Additionally, since claim 8 depends from claim 5, **claim 8** also is not anticipated by, is not obvious from, and is patentable over *Okabe, et al.* for the same reasons.

Rejections under 35 USC 103(a):

Applicant respectfully traverses the rejection of claims 10 and 19 under 35 USC 102(e) as being unpatentable over *Okabe, et al.*, in view of *Matsumoto, et al.* Dependent claims 10 and 19 depend from independent claims 9 and 14, respectively. However, Applicant respectfully submits, as discussed above, that independent claims 9 and 14 are not anticipated by, are not obvious from, and are patentable over *Okabe, et al.*, since the reference does not teach or fairly suggest capturing images of a semiconductor wafer at points of interest proximate to an edge of the semiconductor wafer as claimed. Additionally, *Matsumoto, et al.* does not cure the deficiencies in *Okabe, et al.* Therefore, Applicant respectfully submits that claims 10 and 19 are not anticipated by, are not obvious from, and are patentable over *Okabe, et al.* in view of *Matsumoto, et al.*, since the references do not teach or fairly suggest capturing images of a semiconductor wafer at points of interest proximate to an edge of the semiconductor wafer as claimed.

Allowable Subject Matter:

Applicant respectfully thanks the Examiner for indicating that claims 4, 6, 7, 11, 13 and 15-18 contain allowable subject matter. In view of the above amendments and remarks, however, claims 4, 6, 7, 11, 13 and 15-18 have not been rewritten in independent form, since Applicant respectfully submits that claims 4, 6, 7, 11, 13 and 15-18 depend from allowable base claims.

For the reasons specifically discussed above, and others, it is believed that pending claims 1-14 define patentable subject matter. Reconsideration of the previous rejections as they might apply to the pending claims is therefore respectfully requested. Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

Respectfully submitted,

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Date

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